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2609	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/829,495	TAYLOR ET AL.	
	Examiner	Art Unit	
	Ashley L. Shivers	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 22 April 2004 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

--page 2 lines 13 the verb "be" should be removed after "may".

--page 3 lines 1-2 repeats "while troubleshooting a network circuit" stated at the beginning of the same sentence.

-- page 3 lines 16-17 repeat "It is with respect to these considerations and others that the present invention has been made" stated in the previous sentence.

-- page 4 line 28 the "to" before "utilized" should be removed.

-- page 10 line 3 the "to" should be removed after for.

-- page 12 line 7 "with" should be changed to "which".

-- page 12 line 22 the figure no. is missing after "FIG."

-- page 15 line 4 the "is" should be removed after failure.

Appropriate correction is required.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the DLCIs, VPI/VCI, PVCs, and SVCs must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1 and 3-12 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 4-6, 25-31, and 33-41 of copending **Application No. 10/745047**, hereinafter referred to as '047. Although the conflicting claims are not identical, they are not patentably distinct from each other.

Regarding claim 1, '047 discloses a method for fail-safe renaming of logical circuit identifiers for rerouted logical circuits in a data network, the method comprising **(Claim 1 Preamble)**:

providing a network management module (**Claim 31**) for renaming a first logical circuit identifier for a first logical circuit in the data network to a second logical circuit identifier for a second logical circuit utilized for rerouting data from the first logical circuit in the data network (**Claim 1**); and

renaming a logical circuit label for the first logical circuit in a logical element module in communication with the network management module, wherein the renamed logical circuit label is utilized to indicate that the logical circuit data from the first logical circuit has been rerouted (**Claim 1**).

Regarding claim 3, the '047 further discloses the method of claim 1, wherein the second logical circuit is a logical failover circuit in the data network (**Claim 42**).

Regarding claim 4, '047 further discloses the method of claim 1, wherein the second logical circuit is a currently unused logical circuit in the data network (**Claim 4**).

Regarding claim 5, '047 further discloses the method of claim 1, wherein the first logical circuit identifier is a data link connection identifier (DLCI) (**Claim 5**).

Regarding claim 6, '047 further discloses the method of claim 1, wherein the second logical circuit identifier is a data link connection identifier (DLCI). (**Claim 6**).

Regarding claim 7, '047 further discloses the method of claim 1, wherein the first logical circuit identifier is a virtual path/virtual circuit identifier (VPI/VCI) (**Claim 25**).

Regarding claim 8, '047 further discloses the method of claim 1, wherein the second logical circuit identifier is a virtual path/virtual circuit identifier (VPI/VCI) (**Claim 26**).

Regarding claim 9, '047 further discloses the method of claim 1, wherein the first and second logical circuits are permanent virtual circuits (**Claim 27**).

Regarding claim 10, '047 further discloses the method of claim 1, wherein the first and second logical circuits are switched virtual circuits (**Claim 28**).

Regarding claim 11, '047 further discloses the method of claim 1, wherein the data network is a frame relay network (**Claim 29**).

Regarding claim 12, '047 further discloses the method of claim 1, wherein the data network is an asynchronous transfer mode (ATM) network (**Claim 30**).

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

3. Claims 2 and 13-22 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of copending **Application No. 10/745047** in view of copending **Application No. 10/745117**, hereinafter referred to as '117 and in further view of Ashton et al (**U.S. Patent No. 6,181,679**) hereinafter referred to as Ashton.

Regarding claim 2, '047 further teaches the method of claim 1, wherein renaming a first logical circuit identifier for a first logical circuit in the data network to a second logical circuit identifier for a second logical circuit utilized for rerouting data from the first logical circuit in the data network (**Claim 1**), comprises:

provisioning the second logical circuit in the network device for rerouting the data from the first logical circuit (**Claim 1**), wherein provisioning the second logical circuit includes assigning the second logical circuit identifier to identify the second logical circuit (**Claim 1**); and

renaming the first logical circuit identifier to the second logical circuit identifier (**Claim 1**).

'047 fails to teach of accessing the network device for routing data over the first logical circuit.

'117 teaches of accessing a network device provisioned for routing data over the first logical circuit in the data network (**Claim 13**);

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention, to modify the method of '047 to include accessing a network device for routing data over the first logical circuit taught by '117 in order to show how the circuit information is obtained.

'047 fails to teach of deleting the first logical circuit upon detecting failure.

Ashton teaches of deleting the first logical circuit in the network device upon detecting a failure in the first logical circuit (**See col. 3 lines 22-24**);

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention, to modify the method of '047 to include deleting the first logical circuit taught by Ashton in order to remove the failure and prevent it from being transmitted again.

Regarding claim 13, '047 further teaches a system for fail-safe renaming of logical circuit identifiers for rerouted logical circuits in a data network (**Claim 1**), the system comprising:

identifying a failure in the logical circuit (**Claim 41**);

establishing the communication path for the logical failover circuit to reroute the data from the failed logical circuit (**implied by claim 1 in that if there is rerouting then there has to be an alternative path**);

assigning a logical failover circuit identifier to identify the logical failover circuit (**Claim 31**);

renaming a logical circuit identifier for the failed logical circuit to the logical failover circuit identifier in the network database (**Claim 41**); and

renaming a logical circuit label for the failed logical circuit in the logical element module (**Claim 41**), wherein the renamed logical circuit label is utilized to indicate that the logical circuit data from the failed logical circuit has been rerouted (**Claim 41**).

'047 fails to teach of the network device for establishing the communication paths, a logical element module, and a network management module.

'117 teaches:

a network device for establishing a communication path for a logical circuit and a logical failover circuit in the data network (**Claim 1 and 13**);

a logical element module in communication with the network device for configuring the logical circuit and the logical failover circuit (**Claim 13**); and

a network management module, in communication with the logical element module (**Claim 13**)

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention, to modify the method of '047 to include network device for establishing the communication paths, a logical element module, and a network management module taught by '117 in order to provide the means for establishing the communication paths for the circuits and configuring the circuits for use.

'047 fails to teach of deleting the communication path for the failed first logical circuit.

Ashton teaches of deleting the communication path for the failed logical circuit in the network device (**See col. 3 lines 22-24**);

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention, to modify the method of '047 to include deleting the first logical circuit taught by Ashton in order to remove the failure and prevent it from being transmitted again.

Regarding claim 14, '047 further teaches the system of claim 13, wherein the logical circuit identifier is a data link connection identifier (DLCI) (**Claim 33**).

Regarding claim 15, '047 further teaches the system of claim 13, wherein the logical failover circuit identifier is a data link connection identifier (DLCI) (**Claim 34**).

Regarding claim 16, '047 further teaches the system of claim 13, wherein the logical circuit identifier is a virtual path/virtual circuit identifier (VPI/VCI) (**Claim 35**).

Regarding claim 17, '047 further teaches the system of claim 13, wherein the logical failover circuit identifier is a virtual path/virtual circuit identifier (VPI/VCI) (**Claim 36**).

Regarding claim 18, '047 further teaches the system of claim 13, wherein the logical circuit and the logical failover circuit are permanent virtual circuits (**Claim 37**).

Regarding claim 19, '047 further teaches the system of claim 13, wherein the logical circuit and the logical failover circuit are switched virtual circuits (**Claim 38**).

Regarding claim 20, '047 further teaches the system of claim 13, wherein the data network is a frame relay network (**Claim 39**).

Regarding claim 21, '047 further teaches the system of claim 13, wherein the data network is an asynchronous transfer mode (ATM) network (**Claim 40**).

Regarding claim 22, '047 further teaches a method for fail-safe renaming of logical circuit identifiers for rerouted logical circuits in a data network, the method comprising:

providing a network management module (**Claim 31**) for:

provisioning the second logical circuit in the network device for rerouting the data from the first logical circuit (**Claim 1**), wherein provisioning the second logical circuit includes assigning the second logical circuit identifier to identify the second logical circuit (**Claim 1**); and

renaming the first logical circuit identifier to the second logical circuit identifier (**Claim 1**); and

renaming a logical circuit label for the first logical circuit in a logical element module in communication with the network management module, wherein the renamed logical circuit label is utilized to indicate that the logical circuit data from the first logical circuit has been rerouted (**Claim 41**).

'047 fails to teach of accessing the network device for routing data over the first logical circuit.

'117 teaches of accessing a network device provisioned for routing data over the first logical circuit in the data network (**Claim 13**);

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention, to modify the method of '047 to include accessing a network device for routing data over the first logical circuit taught by '117 in order to show how the circuit information is obtained.

'047 fails to teach of deleting the first logical circuit upon detecting failure.

Ashton teaches of deleting the first logical circuit in the network device upon detecting a failure in the first logical circuit (**See col. 3 lines 22-24**);

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention, to modify the method of '047 to include deleting the first logical circuit taught by Ashton in order to remove the failure and prevent it from being transmitted again.

This is a provisional obviousness-type double patenting rejection.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 1, 2, 5, 6, 9-15, and 18-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Ashton.

Regarding claim 1, Ashton discloses a method for fail-safe renaming of logical circuit identifiers for rerouted logical circuits in a data network, the method comprising **(See col. 7 lines 47-67 and col. 8 lines 1-12; renaming is implied as a substitute would take over the current name of the identifier)**:

providing a network management module **(See col. 3 lines 37-40)** for renaming a first logical circuit identifier for a first logical circuit in the data network to a second logical circuit identifier **(See col. 7 lines 47-67 and col. 8 lines 1-12; renaming is implied as a substitute would take over the current name of the identifier)** for a second logical circuit utilized for rerouting data from the first logical circuit in the data network **(See col. 3 lines 37-43)**; and

renaming a logical circuit label for the first logical circuit in a logical element module in communication with the network management module, wherein the renamed logical circuit label is utilized to indicate that the logical circuit data from the first logical circuit has been rerouted **(See col. 7 lines 47-67 and col. 8 lines 1-12; renaming is implied as a substitute would take over the current name of the identifier)**.

Regarding claim 2, Ashton further discloses the method of claim 1, wherein renaming a first logical circuit identifier for a first logical circuit in the data network to a second logical circuit identifier for a second logical circuit utilized for rerouting data from the first logical circuit in the data network, comprises:

accessing a network device provisioned for routing data over the first logical circuit in the data network (**See col. 3 lines 37-43, col. 7 lines 47-67 and col. 8 lines 1-12**);

deleting the first logical circuit in the network device upon detecting a failure in the first logical circuit (**See col. 3 lines 22-24**);

provisioning the second logical circuit in the network device for rerouting the data from the first logical circuit, wherein provisioning the second logical circuit includes assigning the second logical circuit identifier to identify the second logical circuit (**See col. 7 lines 47-67 and col. 8 lines 1-12; renaming is implied as a substitute would take over the current name of the identifier**); and

renaming the first logical circuit identifier to the second logical circuit identifier (**See col. 7 lines 47-67 and col. 8 lines 1-12; renaming is implied as a substitute would take over the current name of the identifier**).

Regarding claims 5 and 6, Ashton further discloses the method of claim 1, wherein the first and second logical circuit identifiers are data link connection identifiers (DLCI) (**See col. 6 lines 52-55**).

Regarding claims 9 and 10, Ashton further discloses the method of claim 1, wherein the first and second logical circuits are permanent virtual circuits (**See col. 6 lines 3-7**) or wherein the first and second logical circuits are switched virtual circuits (**See col. 6 lines 3-7**).

Regarding claim 11, Ashton further discloses the method of claim 1, wherein the data network is a frame relay network (**See col. 4 lines 55-57**).

Regarding claim 12, Ashton further discloses the method of claim 1, wherein the data network is an asynchronous transfer mode (ATM) network (**See col. 4 lines 57-61**).

Regarding claim 13, Ashton teaches a system for fail-safe renaming of logical circuit identifiers for rerouted logical circuits in a data network, the system comprising:

a network device for establishing a communication path for a logical circuit and a logical failover circuit in the data network (**See col. 3 lines 37-43, col. 7 lines 47-67 and col. 8 lines 1-12**);

a logical element module in communication with the network device for configuring the logical circuit and the logical failover circuit (**See Fig. 4, 32**); and

a network management module (**See col. 3 lines 37-43**), in communication with the logical element module, for:

identifying a failure in the logical circuit (**See col. 3 lines 22-24**);

deleting the first logical circuit in the network device upon detecting a failure in the first logical circuit (**See col. 3 lines 24-27**);

establishing the communication path for the logical failover circuit to reroute the data from the failed logical circuit (**implied in that if there is a failover circuit then there has to be an associated path to communicate over**);

assigning a logical failover circuit identifier to identify the logical failover circuit (**See col. 6 lines 52-55**);

renaming a logical circuit identifier for the failed logical circuit to the logical failover circuit identifier in the network database (**See col. 7 lines 47-67 and col. 8 lines 1-12; renaming is implied as a substitute would take over the current name of the identifier**); and

renaming a logical circuit label for the failed logical circuit in the logical element module, wherein the renamed logical circuit label is utilized to indicate that the logical circuit data from the failed logical circuit has been rerouted (**See col. 7 lines 47-67 and col. 8 lines 1-12; renaming is implied as a substitute would take over the current name of the identifier**).

Regarding claims 14 and 15, Ashton further teaches the system of claim 13, wherein the logical circuit identifier and the logical failover circuit identifier are data link connection identifier (DLCI) (**See col. 6 lines 52-55**)

Regarding claims 18 and 19, Ashton further teaches the system of claim 13, wherein the logical circuit and the logical failover circuit are permanent virtual circuits (**See col. 6 lines 3-7**) or switched virtual circuits (**See col. 6 lines 3-7**).

Regarding claim 20, Ashton further teaches the system of claim 13, wherein the data network is a frame relay network (**See col. 4 lines 55-57**).

Regarding claim 21, Ashton further teaches the system of claim 13, wherein the data network is an asynchronous transfer mode (ATM) network (**See col. 4 lines 57-61**).

Regarding claim 22, Ashton teaches a method for fail-safe renaming of logical circuit identifiers for rerouted logical circuits in a data network, the method comprising:

providing a network management module for:

accessing a network device provisioned for routing data over a first logical circuit in the data network (**See col. 3 lines 37-43, col. 7 lines 47-67 and col. 8 lines 1-12**);

deleting the first logical circuit in the network device upon detecting a failure in the first logical circuit (**See col. 3 lines 24-27**);

provisioning a second logical circuit in the network device for rerouting the data from the first logical circuit (**See col. 3 lines 37-43**), wherein provisioning the second logical circuit includes assigning a

second logical circuit identifier to identify the second logical circuit (**See col. 7 lines 47-67 and col. 8 lines 1-12; renaming is implied as a substitute would take over the current name of the identifier**); and

renaming a first logical circuit identifier to the second logical circuit identifier (**See col. 7 lines 47-67 and col. 8 lines 1-12; renaming is implied as a substitute would take over the current name of the identifier**); and

renaming a logical circuit label for the first logical circuit in a logical element module in communication with the network management module, wherein the renamed logical circuit label is utilized to indicate that the logical circuit data from the first logical circuit has been rerouted (**See col. 7 lines 47-67 and col. 8 lines 1-12; renaming is implied as a substitute would take over the current name of the identifier**).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 3, 4, 7, 8, 16, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ashton in view of Chen et al. **(U.S. PGPub No. 2005/0013242)**, hereinafter referred to as Chen.

Regarding claims 3 and 4, Ashton teaches the method of claim 1, but fails to teach of the second logical circuit being a logical failover circuit and being a currently unused logical circuit.

Chen teaches that the second logical circuit is a logical failover circuit in the data network **(See [0022] lines 3-6)** and the second logical circuit is a currently unused logical circuit in the data network **(See [0022] lines 3-6)**.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention, to modify the method of Ashton to include the second logical circuit being a failover circuit and a currently unused logical circuit taught by Chen in order to provide an existing secondary path for the data to be sent.

Regarding claims 7, 16 and 8, 17, Ashton teaches the method of claims 1 and 13, but fails to teach of the circuit identifiers being VPI/VCI.

Chen teaches that the first and second logical circuit identifiers are virtual path/virtual circuit identifiers (VPI/VCI) **(See [0004] lines 27-32)**.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention, to modify the method of Ashton to include the logical circuit identifiers being virtual path/ virtual circuit identifiers taught by Chen in order to

provide the identification of the circuit and the path that the circuit will take in the ATM network.

Conclusion

8. Any response to this action should be **faxed** to (571)273-8300 or **mailed** to:

Commissioner of Patents,
P.O. Box 1450
Alexandria, VA 223103-1450

Hand delivered responses should be brought to:
Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ashley L. Shivers whose telephone number is (571) 270-3523. The examiner can normally be reached on Monday-Thursday 8:30-7:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Benny Tieu can be reached on (571) 272-7490. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AS

BENNY Q. TIEU
SPE/TRAINER